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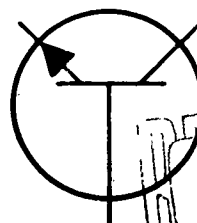
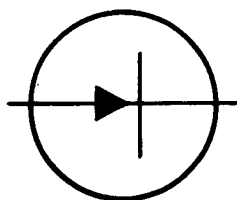


# Westinghouse

## ELECTRIC CORPORATION

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**WESTINGHOUSE ELECTRIC CORPORATION**

1625 K Street  
Washington, D. C.

Third Quarterly Report  
(covering period 1 January to 31 March, 1963)

HIGH CURRENT AND HIGH VOLTAGE  
SILICON CONTROLLED RECTIFIERS

NObsr-87647 Proj. No. SR-0080301 Task No. 9348

NAVY DEPARTMENT  
BUREAU OF SHIPS  
ELECTRONICS DIVISION

**WESTINGHOUSE ELECTRIC CORPORATION**

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ABSTRACT

Both crucible grown and float-zone silicon crystals were received and processed through, at least, the initial stages of device fabrication. Evaluation data on both types of material are presented.

Minor modifications of the basic device structure and encapsulation design are noted.

Sample fabrication directed toward more complete evaluation of the device design and generation of state-of-art samples is discussed. Some problems which arose during this work are described.

Electrical evaluation data on prototype samples (encapsulated) are given.

Delivery of twenty state-of-art samples as per schedule is anticipated.

SECTION IA. PURPOSE

The research and development effort to be conducted under this contract is directed toward the development of a 500-ampere, 500-volt silicon controlled rectifier. Specifications for the device are given in Table I.

TABLE I

Characteristic	Symbol	Condition	Value
Average Forward Current (Min.)	$I_{FB(Av)}$	180 electrical degrees of half sine wave conduction at $T_C = 80^\circ C$ .	500A
Peak Surge Current (Min.)	$I_{FM(Surge)}$	A non-recurrent surge 180 electrical degrees of one-half sine wave conduction immediately preceded and followed by $I_{FB(Av)} = 500A$ at $T_C = 80^\circ C$ .	10,000A
Peak Forward and Peak Reverse Blocking Voltage (Min.)	PFV-PRV	Over the workable temperature range of the device.	500V
Turn-Off Time (Max.)	$t_{off}$	Initially 500A into a resistive load with mounting interface surface at $80^\circ C$ steady state.	30 $\mu sec$
Turn-On Time (Max.)	$t_d$ & $t_r$	Turn-on with a square wave current pulse. $I_{FB(Av)}$ may be limited to 50A through a non-inductive load.	10 $\mu sec$
Rate of Rise of Anode-To-Cathode Voltage (Min.)	$dv/dt$	Test circuit similar to MIL-S-19500/204, Fig. 11 shall be used.	50V/ $\mu sec$

Device encapsulation shall be such that it withstands, by itself, normal shipboard environmental conditions. The package shall be designed to remove heat by conduction through a mounting interface surface to a mating surface. The  $80^\circ C$  mounting surface temperature contemplates water cooling of the heat sink to which the device is attached. The device shall not be designed to contain or directly contact liquid or vapor cooling mediums.

In order to attain the contract objectives, a program has been designed about the following phases:

1. Silicon Material ----- availability and procurement
2. Basic Device Structure --- design and optimization
- 3, Encapsulation ----- design and refinement
- 4, Sample Fabrication ----- experimental and final (in-spec)
5. Device Evaluation ----- equipment design and electrical test
6. Delivery ----- devices and reports

B. GENERAL FACTUAL DATA

During this report period, the following personnel contributed to the project effort for the number of man-hours indicated:

L. Garrison	-----	8 hours
A. Knopp	-----	504 hours
R. Kuehn	-----	476 hours
C. Skooglund	-----	3 hours
B. Denis	-----	4 hours
J. Steinbach	-----	22 hours

C. MATERIAL (Silicon)

A total of 26 inches of crucible grown, 1.25-inch diameter, silicon has been received in this report period. The range of the specifications on this material appears in Table II. The problem of orientation noted in the last quarterly report has been solved simply by reducing the limits of the specification to  $(111) \pm 0.5^\circ$ .

TABLE II

Crucible Grown Silicon Evaluation Data

Diameter -----	1.25 inch
Resistivity -----	19-30 ohm-cm
Resistivity Gradient (across slice) --	1 - 5%
Lifetime -----	20 - 300 microseconds
Dislocation Density -----	0 - 13,000/cm <sup>2</sup>
Lineage -----	None

Approximately five inches (three ingots) of float zone material have been received recently. The range of the specifications on this material appears in Table III.

TABLE III

Diameter -----	1.25 inch
Resistivity -----	17-22 ohm-cm
Resistivity Gradient (across slice) --	1 - 18%
Lifetime -----	40 - 110 microseconds
Dislocation Density -----	20,000 - 60,000/cm <sup>2</sup>
Lineage -----	Excess lineage appeared on the outer edge of one ingot.

The parameters of the float zone material are tolerable. It should be noted that the lifetime is below standard and the dislocation density is somewhat high. Either could impair the electrical parameters of devices made from this material. The material does indicate that excellent progress is being made with the float zone silicon technology. This silicon will be processed in the next quarter. Thus, diffusion and alloying results are not presented in this report.

D. BASIC DEVICE STRUCTURE

The basic device structure has not been changed during this period. The first test results have shown that the required specifications on parameters measured to date can be met; however, the percentage of units which meet all required electrical data cannot yet be established. Therefore, the possibility of further optimization of the basic device structure continues to be a part of the program.

E. ENCAPSULATION

During the reporting period, deliveries of all capsule components were received. Sub-assemblies were made to determine proper encapsulation procedures and to demonstrate that all capsule components could be properly assembled. No difficulties were encountered which indicated a need for modification of the capsule design.

In the second quarterly report, two alternate base styles for the device were discussed. A complete comparison of the two designs has not been made. However, preliminary test data of the thermal resistance from case-to-sink, when mounted on an air cooled plate, indicates the two designs are almost identical. If subsequent evaluation does not indicate any substantial difference in thermal characteristics of the two designs, the choice of the final design will be based on compatibility of the structure with the fabrication process and/or the preferred mounting technique.

Three alloys are under consideration for the base. Two have been received to date. The final base design will incorporate that alloy which provides optimum thermal and mechanical characteristics.

It has been decided to modify the capsule seal by threading the cathode terminal. This will allow standard stud-to-cable connectors to be used

for the cathode power connection. The suggestion of a modified solid ceramic top seal to be used in place of the metal cap type of ceramic seal has been shelved. Although the modified seal possesses some advantages, tooling and delivery would delay the encapsulation phase of the project at least three months. Moreover, the present design satisfies all mechanical and electrical design features required.

The basic overall design of the encapsulation components are fixed with the exception of the possible change in base material and/or geometry.

#### F. SAMPLE FABRICATION

##### 1. Silicon Preparation

The same operations of slicing, lapping and etching were followed as described in the second quarterly report.

##### 2. Diffusion

The sealed quartz ampoule technique has been followed in the same way as described in the second quarterly report. During this period, two diffusion runs have been carried out. Gallium surface concentrations have been held slightly above  $1 \times 10^{18} \text{ cm}^{-3}$  in order to compare results with previous diffused silicon, the  $C_s$  of which had been slightly below the above-mentioned value. Junction depths were in the required range.

The diffused wafers of the first run could not be processed due to surface contamination which could not be removed satisfactorily. Silicon diffused in the second run showed no contamination; however, leakage currents of the blocking voltages were relatively high after alloying. This resulted in poor temperature dependence of the breakover voltage, although small area "control samples" yielded good results. It is believed that the contamination problem had not truly been eliminated and probably originated in the vacuum sealing system. Effort has already been spent to

exclude undesired impurities in the system.

### 3. Alloying

The component parts which comprise the fusion assembly and the alloying technique per se have not been changed during this period. A total of thirty-four elements were fused. Fifteen of these are still in process; six had a breakover voltage less than 100 volts at 125°C; six failed in alloying due to poor vacuum; two were processed with a smaller gold-antimony emitter; and the remaining five were encapsulated, having yielded reasonable blocking voltages at 125°C. Of the total of thirty-two encapsulated units (see further below) twenty-seven were elements processed in the last period.

Two control elements were made in this period. All had forward and reverse voltages in excess of 500 volts at 125°C.

### 4. Surface Treatment

With the availability of 1.25 inch OD silicon, improved control of the surface contour can be achieved. No unit is encapsulated without being temperature cycled many times to insure stable blocking characteristics. Results show that the stability of the unit to date has been excellent.

### 5. Encapsulation

During this period all component parts were received. Thirty-two state-of-art samples were encapsulated using the stud-mounted capsule described in the first quarterly report. Problems resolved were in-line test procedures, welding schedule for the hermetic seal, and an enlarged weld chamber to accept the large capsule. One problem still unsolved is the pinch-off weld of the gate tube. On the present seal, the gate tube ID is considerably larger than the OD of the silver gate wire. The initial result was about 30% "leakers." On the state-of-art samples, the end

of the gate tube was therefore brazed if the unit indicated any leak. This resulted in 100% hermetic seals. Several possibilities are being investigated to eliminate this problem. Figure 1 shows a fully encapsulated unit.

## G. DEVICE EVALUATION

### 1. Heat Sink Design

Power loss for the 500 ampere silicon controlled rectifier was calculated previously at 750 watts under rated conditions. To dissipate this quantity of heat, an efficient heat sink is required. The second quarterly progress report, covering the period 10 October 1962 to 31 December 1962, described a rosette water passage pattern heat sink. Figure 2 shows a finished model of the heat sink described. A sample of the 500 ampere device is shown mounted on the water cooled fixture in Figure 3. All device power tests will be performed on this fixture.

### 2. Device Test Data

Device design characteristics were calculated and verified by measurements.

Three prototype devices were assembled for preliminary evaluation prior to manufacture of the state-of-art samples. Primary interest was directed to determine the current carrying and voltage blocking capabilities of the basic device wafer under load conditions. Further, measurements were made to determine the trend of the forward junction breakover voltage as a function of junction temperature.

The forward current test is performed by mounting the test device on the

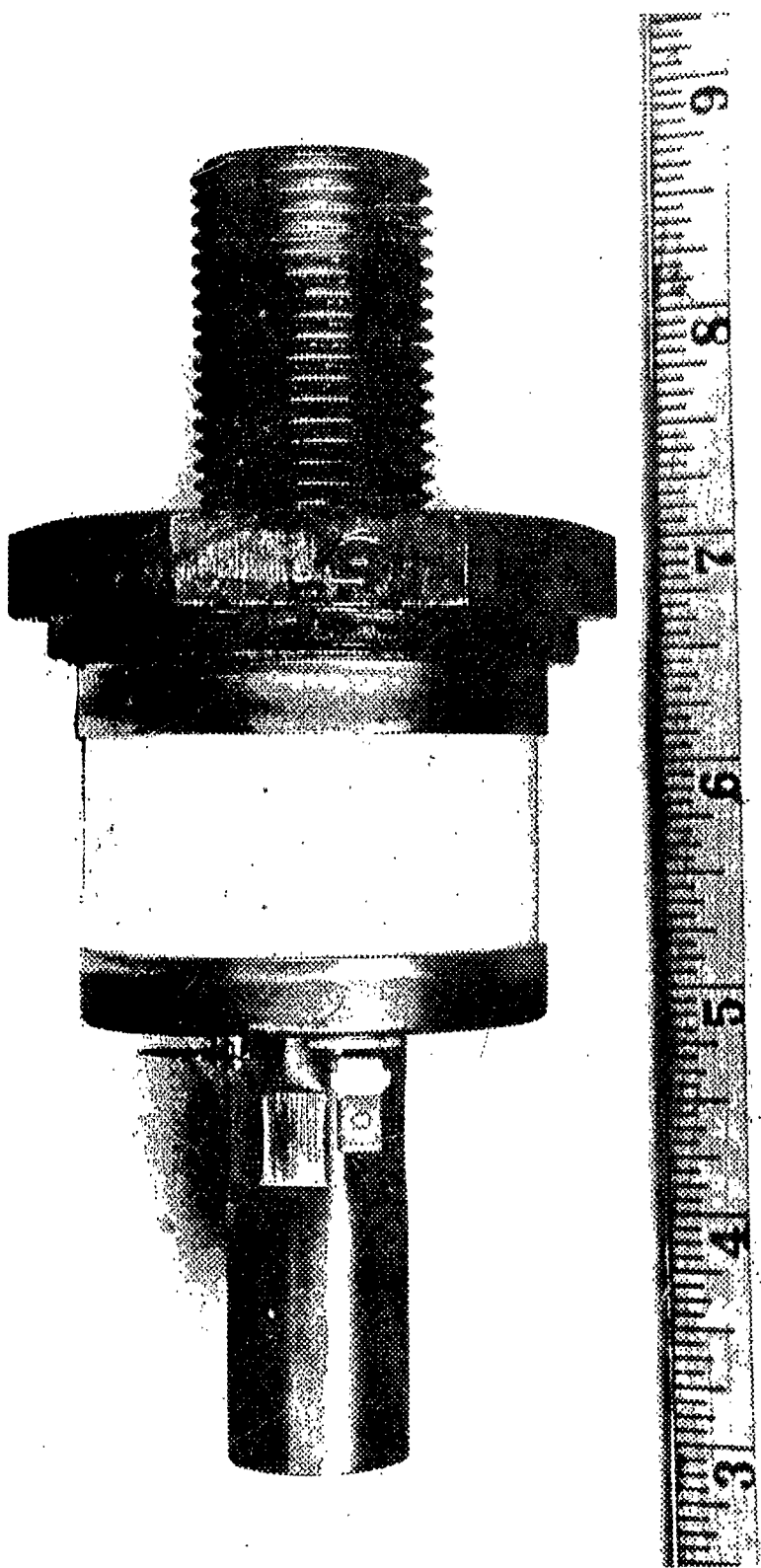


Figure 1. Encapsulated 500 Ampere Silicon Controlled Rectifier

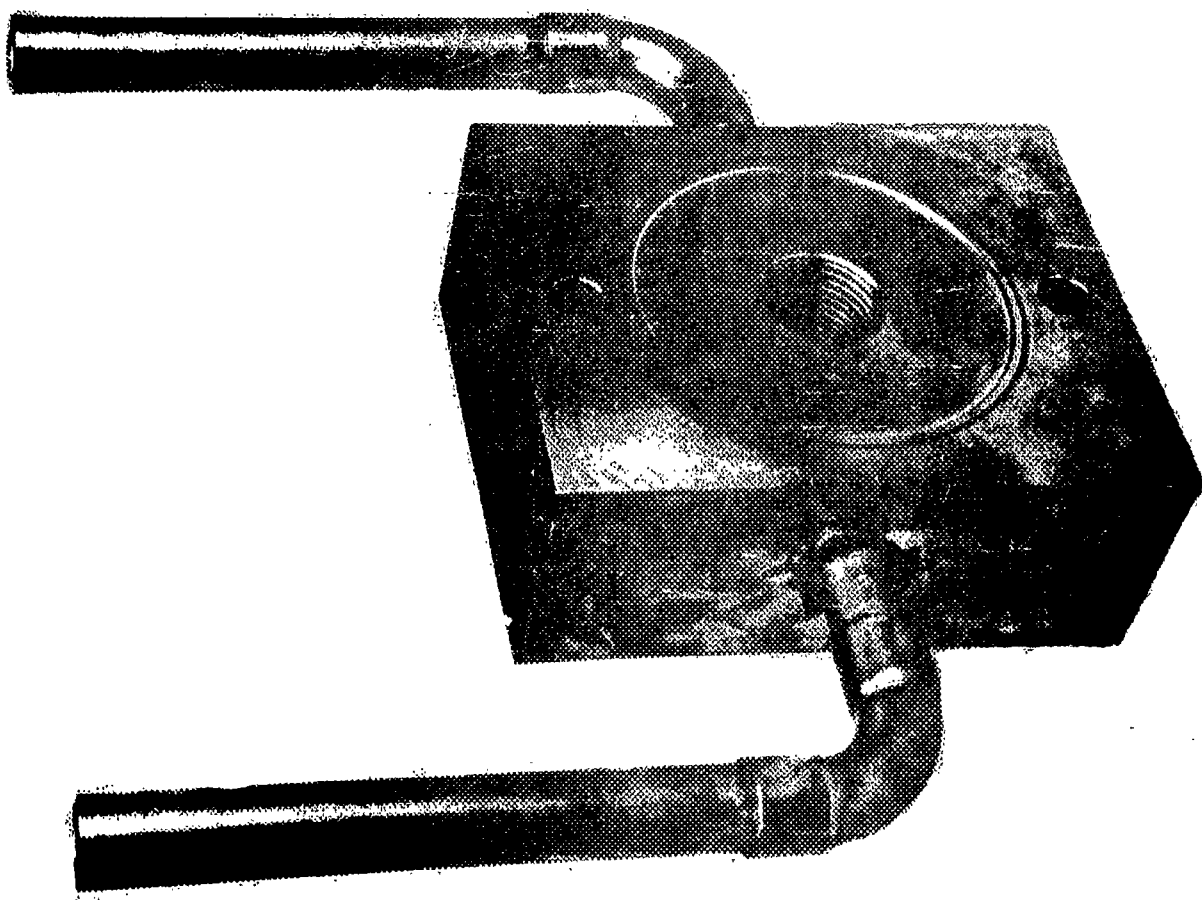


Figure 2. Model Rosette Water Passage Pattern Heat Sink

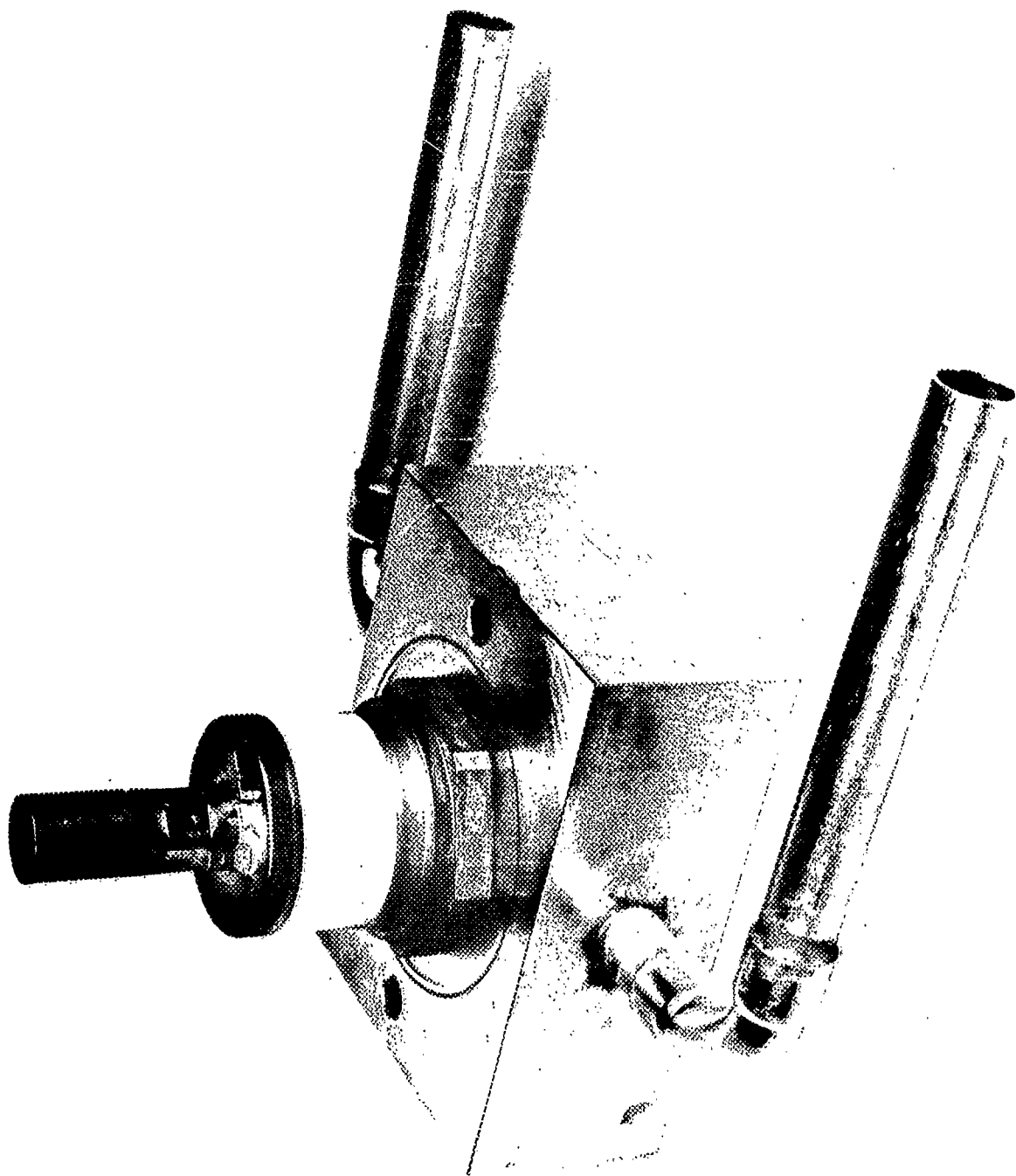


Figure 3. 500 Ampere Silicon Controlled Rectifier Mounted On Heat Sink

water cooled heat sink. The device is gate triggered "on" and forward current (500 amperes average half wave) passed for a conduction period of 180°. During the blocking half cycle, forward anode-to-cathode voltage is applied. The peak voltage applied corresponds to the voltage class for a junction temperature of 125°C. Characteristic wave shapes for this test are shown in the first quarterly report for the period 29 June to 30 Sept., 1962.

Load test data for the three prototype devices is shown in Table IV. The case temperatures recorded were obtained by regulating the rate of cooling water flow through the heat sink while the device conducts forward current.

Two devices ( HH11 and 20NN) successfully carried 500 amperes average half wave forward current while retaining a forward blocking characteristic. The third device (12NN) passed only 270 amperes forward current at  $T_C = 56^\circ\text{C}$ , indicating a high thermal resistance, junction-to-case. However, a larger number of units have to be tested to establish the average thermal impedance value. These results will dictate the direction of effort in optimizing the device and encapsulation designs to meet the complete specifications of the contract.

Peak forward voltage drops were recorded at peak currents of 500, 1000, and 1500 amperes.

The recorded test data and plotted curves for the breakover voltage as a function of junction temperature of the three test devices are shown in Table V and Figure 4, respectively. The curves shown are typical for silicon controlled rectifiers.

It should be noted that these data represent the first test data on encapsulated devices. At the time of this writing, the state-of-art samples

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are being tested. These data will provide a truer picture of the state-of-art device characteristics.

TABLE IV

Load Test Data

(Pre-assembly state-of-art devices)

<u>Unit No.</u>	<u>V<sub>FB</sub></u> (Volt)	<u>I<sub>F</sub></u> (Amp)	<u>T<sub>C</sub></u> (°C)	<u>V<sub>P</sub>/I<sub>P</sub></u> (volt/amp)	<u>V<sub>P</sub>/I<sub>P</sub></u> (volt/amp)	<u>V<sub>P</sub>/I<sub>P</sub></u> (volt/amp)
HH11	400	500	80°	0.96/500	1.04/1000	1.1/1500
12NN	400	270	56°	0.98/500	1.05/1000	1.12/1500
20NN	500	500	54°	1.0/500	1.1/1000	1.18/1500

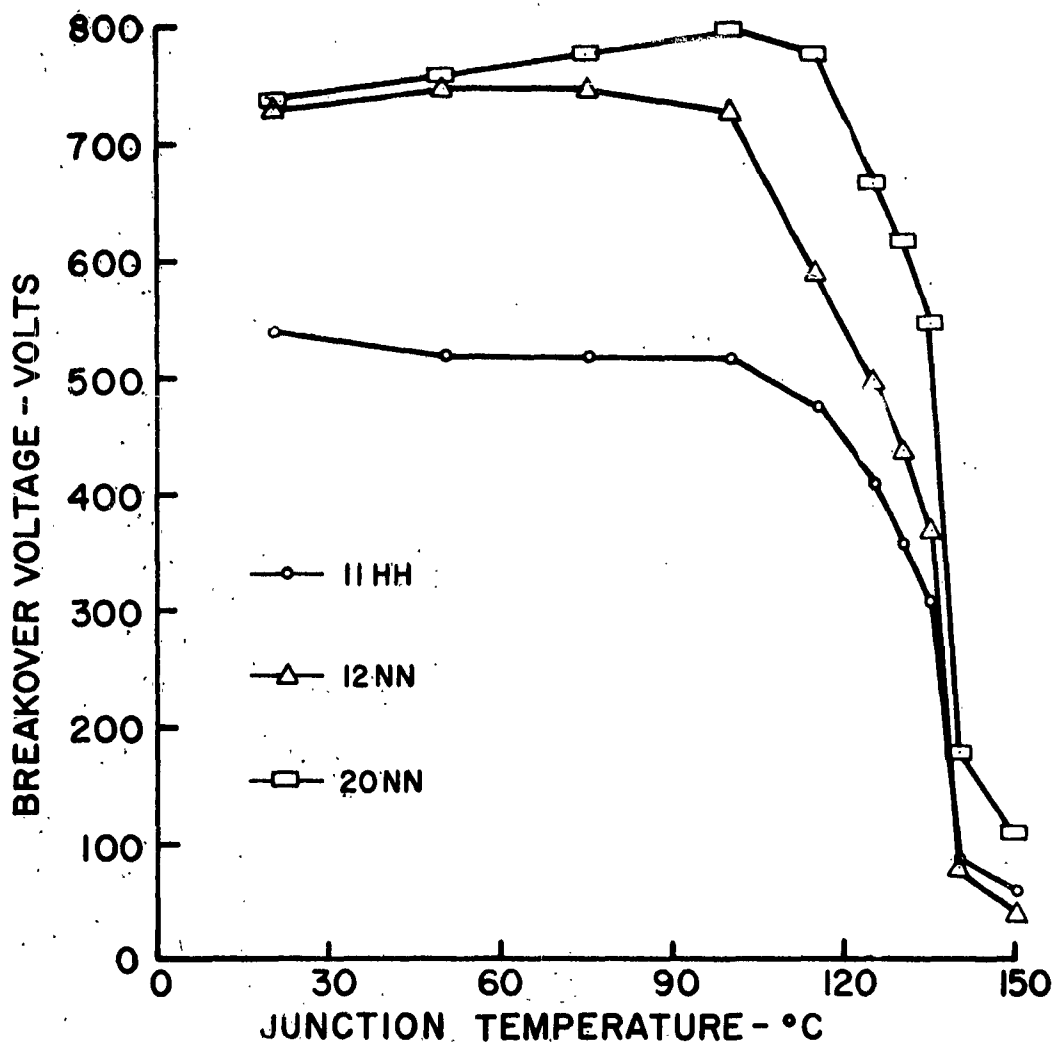
TABLE V

V<sub>BO</sub> vs. Junction Temperature Data

(Pre-assembly state-of-art devices)

V<sub>BO</sub> - Volts

<u>Unit No.</u>	<u>T<sub>J</sub></u>	<u>20.5°C</u>	<u>50°C</u>	<u>75°C</u>	<u>100°C</u>	<u>115°C</u>	<u>125°C</u>	<u>130°C</u>	<u>135°C</u>	<u>140°C</u>	<u>150°C</u>
HH11		540	520	520	720	480	410	360	310	90	60
12NN		730	750	750	730	590	500	440	370	80	40
20NN		740	760	780	800	780	670	620	350	180	110



**Fig. 4 Breakover Voltage as a Function of Junction Temperature**

H. DELIVERY

The twenty state-of-art samples are expected to be delivered at the time indicated by the contract schedule.

J. CONCLUSIONS

It appears that the silicon supply problem anticipated early in the contract is resolved. As expected, technological progress in both crucible grown and float-zone material has kept pace with device development.

The basic device structure employed in work to date indicates that electrical performance (as far as evaluation has progressed) is satisfactory.

Initial thermal data on the base design (stud vs. flat bottom) show little reason to prefer one over the other.

Sample fabrication continued on schedule such that the twenty state-of-art devices should be available for delivery by 30 April, 1963.

Preliminary encapsulated device evaluation data indicate that the state-of-art device characteristics will be appropriate for this stage of the overall program.

SECTION II

A. PROGRAM FOR NEXT INTERVAL

The first third of the next period will be devoted primarily to completing the state-of-art devices for delivery. After this, emphasis will shift to more complete electrical and thermal evaluation of encapsulated units such that all (or most) of the electrical specifications can be checked as per contract requirements. Analysis of this information will be made to determine whether or not the basic device structure and/or encapsulation design requires further modification.

Fabrication of devices will continue to permit refinement of process techniques and evaluation of design changes.

B. PROJECT PERFORMANCE AND SCHEDULE

See Figure 5.

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## Project Performance and Schedule

Project No. SR-0080301

Task No. 9348

Contract No. NObsr-87647

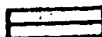
Date: 30 April, 1963

Period Covered: 1/1/63 to 3/30/63

Period Covered: 1/1/63 to 3/30/65																				
	1962					1963												1964		
PHASE	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F
1. MATERIALS (Silicon)																				
Availability survey																				
Procurement to specification																				
2. BASIC DEVICE STRUCTURE																				
Preliminary design studies																				
Optimization																				
Design fixed																				
3. ENCAPSULATION																				
Preliminary design studies																				
Refinement																				
Design fixed																				
4. SAMPLE FABRICATION																				
Experimental studies																				
State-of-art samples																				
Final device samples																				
5. DEVICE EVALUATION																				
Test equipment design																				
Prototype sample evaluation																				
Final device evaluation																				
6. DELIVERY																				
State-of-art samples																				
Final device samples																			50	
Interim engineering reports														X		X				
Final engineering report																				X



Work Performed



Schedule of projected operation

### Estimated Completion in Percent of Total Effort Anticipated by Phase

1. Materials -----60%
2. Basic Device Structure -60%
3. Encapsulation -----70%

4. Sample Fabrication - 25%
5. Device Evaluation--- 35%
6. Delivery (samples) - 0%

Figure 5